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(54) Multilayer wiring structure including via holes

(57) The semiconductor device according to the present invention includes a first wiring formed on a first insulating film, a second insulating film provided on the first wiring, a second wiring provided on the second insulating film, and a plurality of via holes for electrically connecting the first wiring and the second wiring where the first wiring and the second wiring intersect, provided in a via hole formation region, wherein the first wiring is divided in the via hole formation region into a first branch wiring and a second branch wiring, and the widths of the first branch wiring and the second branch wiring are respectively 7 μm or less.

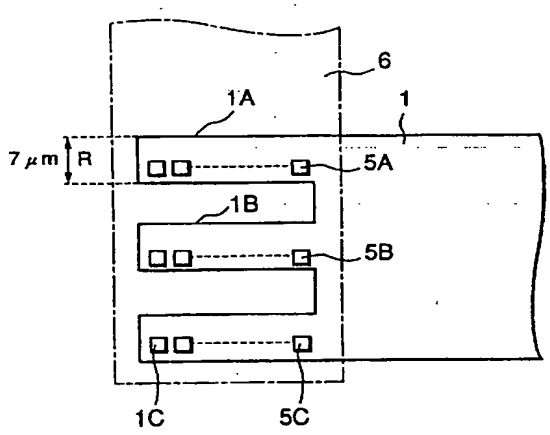

FIG. 5

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BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned and other objects, features and advantages of this invention will become more apparent by reference to the following detailed description of the invention taken in conjunction with the accompanying drains, wherein:

Fig. 1 is a plane view showing a conventional through hole section connecting the first wiring and the second wiring;
Fig. 2 is a sectional view along the line A-A in Fig. 1;
Fig. 3 is a sectional view showing another example of the conventional via hole section;
Fig. 4 is a plan view showing the intersection part of the wirings for describing the problems in the conventional device;
Fig. 5 is a plan view for describing a first embodiment of this invention;
Fig. 6 is a plan view for describing a second embodiment of this invention;
Fig. 7 is a plan view for describing a third embodiment of this invention; and
Fig. 8 is a sectional view for describing this invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Fig. 5, a first embodiment of this invention will be described. The feature of this invention resides in the wiring shape of the portion being the region where a first wiring 1 and a second wiring 6 intersect and where a plurality of via holes for electrically connecting the first wiring 1 and the second wiring 6 are connected. As shown in Fig. 5, a plurality of via hole trains 5A, 5B, and 5C are formed. The shape of the end section of the first wiring 1 is that of a comb which is formed by connecting all of a first branch wiring 1A, a second branch wiring 1B, and a third branch wiring 1C having their respective through hole trains in the region outside a via hole formation region. With such a shape, the distance from the respective via hole trains to either edge of the first wiring 1 can be represented by multiples of the width R of the branch wiring.

The following test was carried out for respective cases of 5, 7, and 10 μm for the branch wiring width R of the first wiring 1.

When an oxide film (with a thickness of about 600 nm) is formed on the patterned first wiring 1, a ruggedness corresponding to the patterning of the first wiring 1 was formed on the surface of the oxide film. When the oxide film was coated with silica solution subsequently, it was confirmed that the silica solution did not stay on the protruded parts because of the surface tension of the silica solution.

When the width of the branch wiring was chosen to be 10 μm, considerable amount of the silica solution stayed on the protruded parts formed by the oxide film deposited on the wiring. Since the complete removal by etch-back of that amount of silica would lead to a problem on the flatness of the surface, it was not practical to remove all of silica from the surface.

When the width of the branch wiring was chosen to be 7 μm, a small amount of silica solution stayed on the protruded parts formed by the oxide film deposited on the wiring. It was found that flatness of the surface was not much affected even if that amount of silica was removed by etch-back.

When the width of the branch wiring was selected to be 3 μm, little silica solution stayed on the protruded parts formed on the oxide film deposited on the wiring. Accordingly, flatness of the surface was not at all affected even if the surface was subjected to etch-back.

As is clear from the above results, it was found that even if the surface is coated with silica solution, not much silica solution remains on the protruded parts owing to the surface tension of the silica solution provided that the width of the branch wiring R is restricted to 7 μm or less.

In the first embodiment shown in Fig. 5, only a small amount of silica that can be etched back will remain on the branch wiring regions that are connected to the via holes provided that the width R of the plurality of branch wirings is chosen to be 7 μm or less. Accordingly, the effect of the silica film in the opening of the via holes can be eliminated. It should be noted that the width of the branch wiring depends on the width of the via hole, and it is necessary to have the width of the branch wiring which is at least twice the width of the through hole. For example, when the width of the via hole is 0.5 μm, the width of the branch wiring of 1 μm or more is necessary.

Next, referring to Fig. 5 and Fig. 8, the production of the device will be described. First, after the formation of a conductive film, consisting of aluminum, tungsten, polycrystalline silicon or a silicide, to a thickness of 300 - 500 nm on an insulating film 10, consisting of an oxide film or the like formed on a semiconductor substrate, the first wiring 1 having a shape as shown in Fig. 5 is formed by patterning. Next, a plasma oxide film 2 is formed to a thickness of about 600 nm at a low temperature (about 400°C), considering the melting point of the first wiring, as an insulating film to avoid the contact between the silica film and the first wiring 1. Next, the entire surface coated with silica solution is heated to 300 - 400°C to form a silica film 3 in order to relax the level difference 7 created as a result of the formation of the first wiring 1. At this time, the unwanted silica film 3 remaining on the plasma oxide film 2 above the wiring 1 is thinned out or removed by etch-back. The coating silica solution on the comb teeth 1A, 1B, and 1C at the end section of the first wiring 1 flows into the spaces (lower portions) between the patterns, so that little silica film 3 is formed on the comb teeth. Even if the silica film is formed to a small extent, it will be removed completely by the etch-back.

Next, a plasma oxide film 4 is formed again at a low

said second branch wiring is larger than about twice the width of said via hole.

9. In a semiconductor device including a first wiring and a second wiring electrically connected via an insulating film to said first wiring by means of a plurality of via holes, the semiconductor device characterized in that said plurality of via holes include a first through hole train and a second through hole train, said first wiring is connected to said first via hole train and said second via hole train respectively, and said first wiring has at least one punched part in the region between said first via hole train and said second via hole train.

10. The semiconductor device as claimed in claim 9, wherein said punched part exists in a plural number.

11. The semiconductor device as claimed in claim 9, wherein the width of said first branch wiring and said second branch wiring is 7 μm or less.

12. The semiconductor device as claimed in claim 11, wherein the width of said first branch wiring and said second branch wiring is greater than about twice the width of said via hole.

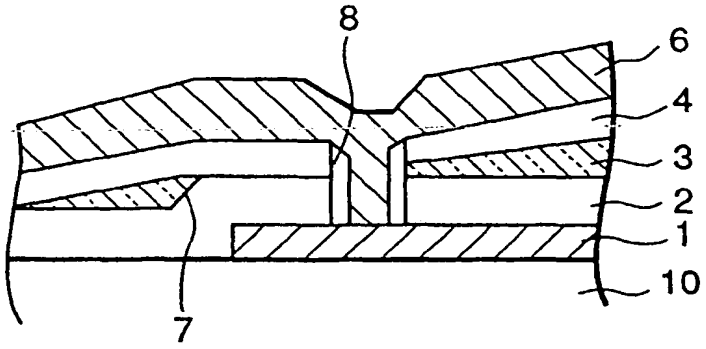

FIG. 3 PRIOR ART

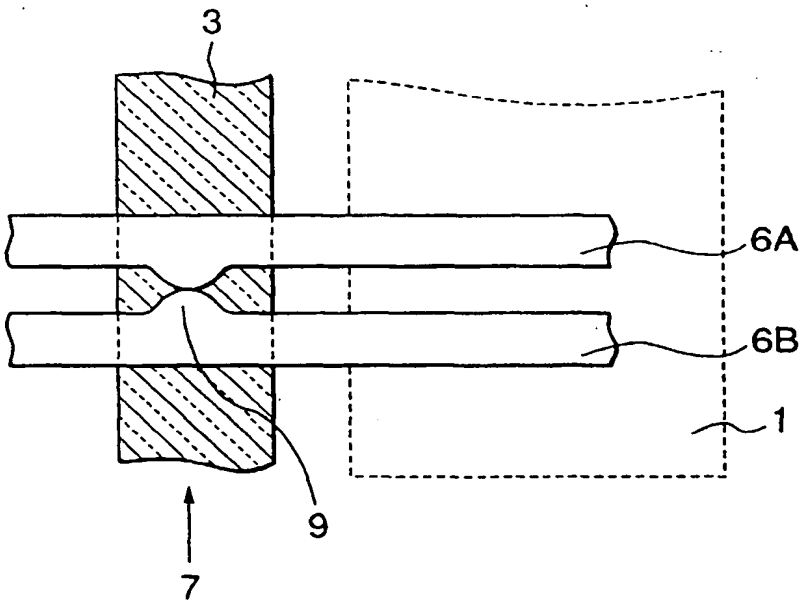

FIG. 4 PRIOR ART

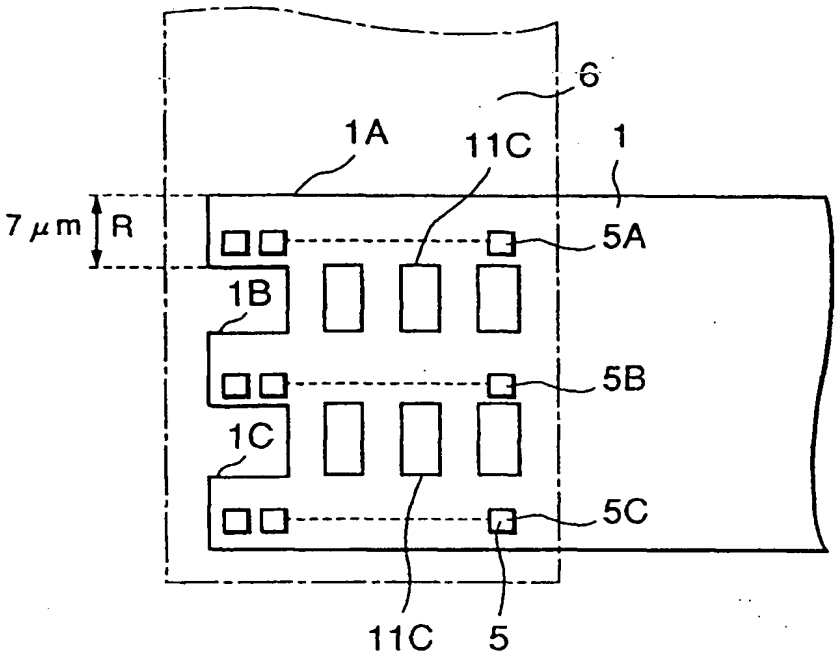

FIG. 7

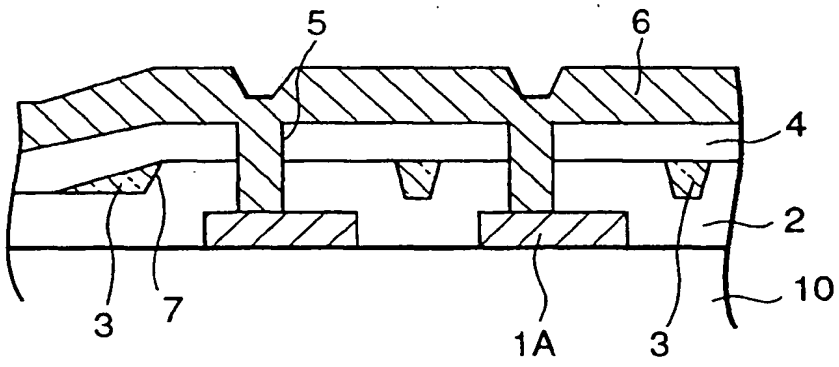

FIG. 8